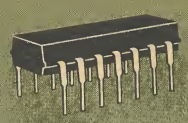
SIGNETICS NE800A-SERIES

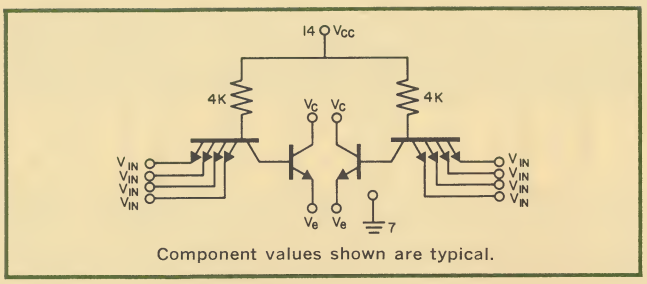
TTL HIGH SPEED INTEGRATED CIRCUITS FOR MILITARY GSE AND HIGH PERFORMANCE COMMERCIAL/INDUSTRIAL APPLICATIONS



AUGUST 1966

NE800A-SERIES

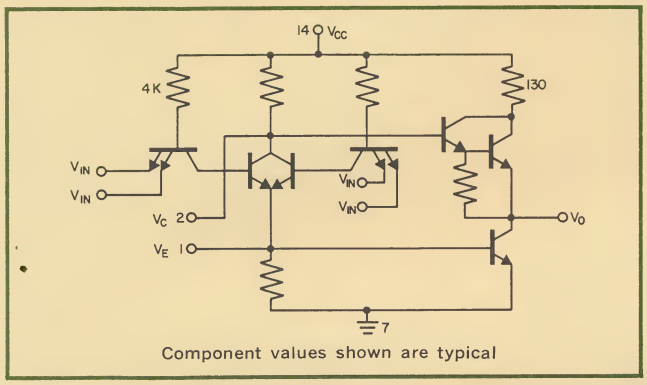
SIGNETICS CORPORATION • 811 EAST ARQUES AVENUE, SUNNYVALE CALIFORNIA • TEL: (408) 739-7700 • TWX: (910) 339-9220



Component values shown are typical.

NE806A

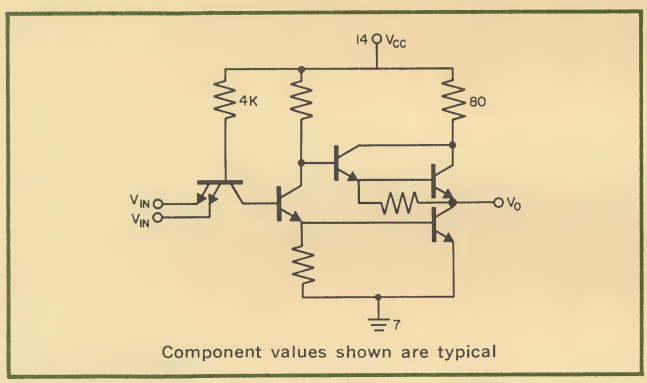
The NE806A dual 4-input gate expander is designed for use with the NE840A Exclusive-OR gate. It serves to increase the number of AND input terms to that element. The inputs of the NE806A represent one DC load. No more than four NE806A expanders may be tied to expansion input of an NE840A.



Component values shown are typical

NE840A

The NE840A is a dual AND/NOR gate in which one of the two NOR gates is expandable. The AND/NOR function readily implements Exclusive-OR in logic. Connection of an NE806A to the expand NOR gate in NE840A has the same function as do the built gates of the NE840A, and simply increases the number of inputs AND function.



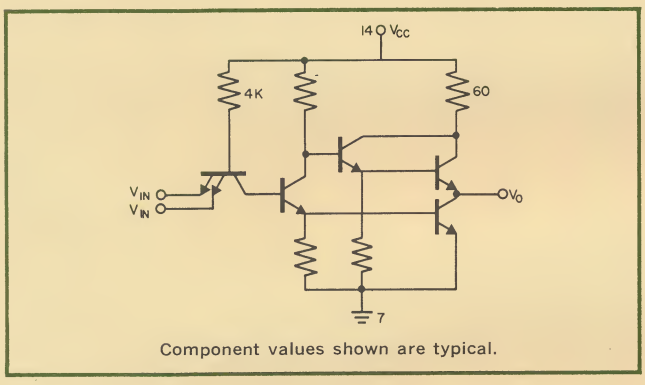
Component values shown are typical

NE808A, NE816A, NE870A, NE880A

These gate elements provide the following functions:

NE808A: Single 8-input NAND **NE870A:** Triple 3-input
NE816A: Dual 4-input NAND **NE880A:** Quad 2-input N

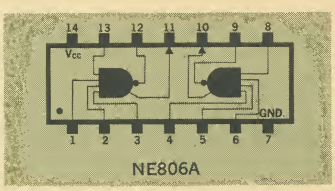
All of these gates utilize multiple emitter transistor (MET) and push-pull or totem pole outputs. They therefore provide high speed and high capacitive drive capability. The input structure is so designed that input voltage latch proble characterize many TTL gates are eliminated. Propagation time, and fall-time are relatively independent of load. input in this group constitutes one DC load.

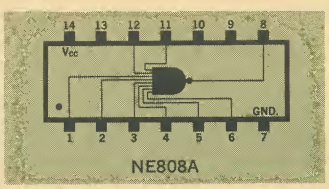


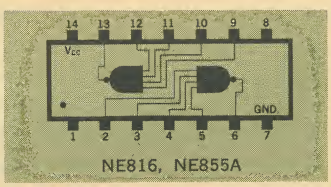
Component values shown are typical.

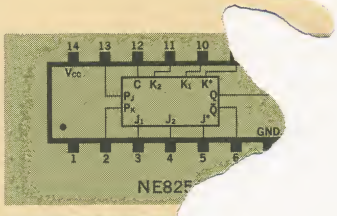
NE855A

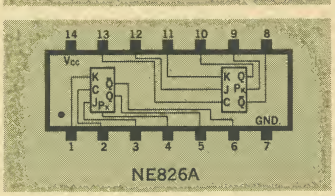
The NE855A is a dual 4-input power NAND gate intended for driving clock lines or other high capacitance loads. similar to that of the basic NAND gates in the NE featuring multiple emitter input transistors and a totem Large geometry transistors are used in the output to pr current capability, and a pull-down resistor provides standby current to enhance switching speed. The NE8 used to drive lamps or other display elements.

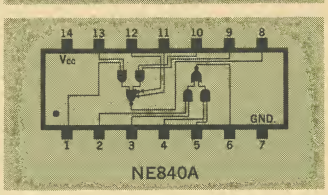


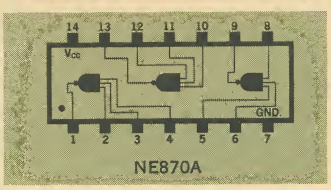


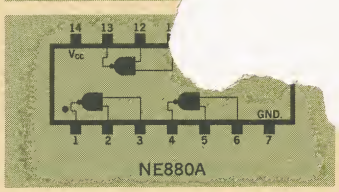




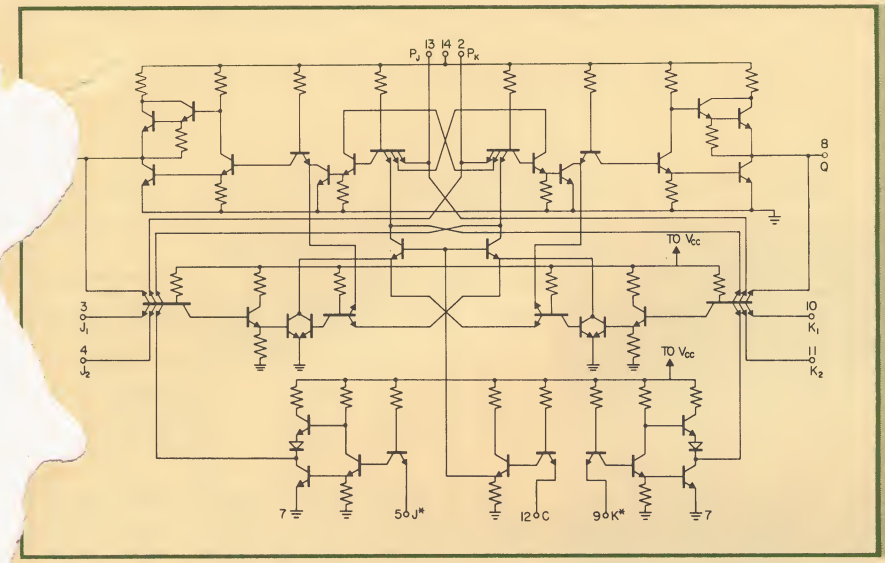








NE825A



TRUTH TABLE

SYNCHRONOUS

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$J=J_1, J_2, \overline{J}^*$, $K=K_1, K_2, \overline{K}^*$

ASYNCHRONOUS

P_J	P_K	Q_{n+1}
0	0	*
1	0	0
0	1	1
1	1	Q_n

*Both outputs low

The NE825A is a single DC clocked flip-flop with gated J, K inputs. Asynchronous preset and clear lines are also provided.

This device responds to the leading edge (positive going) of the clock input. Logical lock-out of the logic inputs prevents more than one ansition of the flip-flop per clock pulse. The required clock-pulse orm is a positive going pulse at least 15 ns wide at the 2 volt with a rise and fall time of less than 150 ns.

nternal 3-input NAND gates are provided at the logic inputs to lement. The NE825A has three J and three K logic inputs, one each, J* and K*, being an inverting input. The J input is enabled hen both J_1 and J_2 are logical ONE and J* is logical ZERO. the K input is enabled only when K_1 and K_2 are logical K* is logical ZERO.

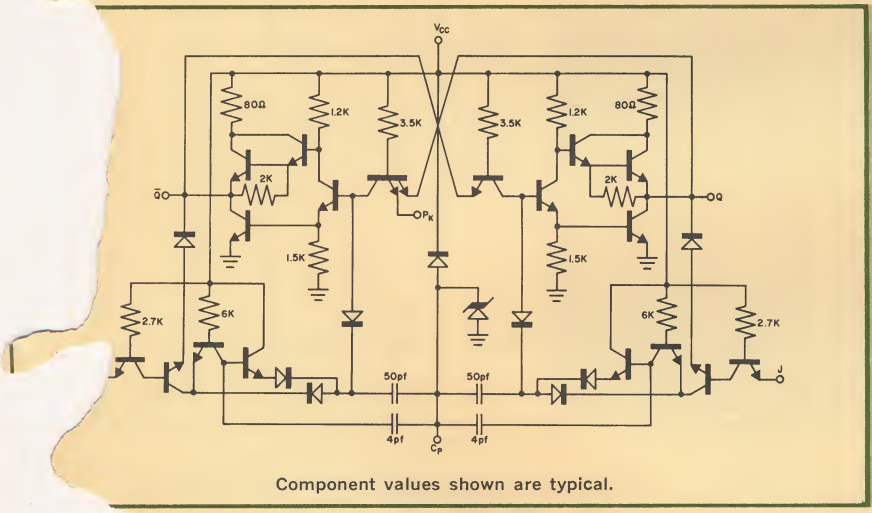
els to the J, K inputs should be stabilized at a logical ONE or ZERO level 10 ns before the clock pulse and should remain stable for 10 ns after the rise of the clock pulse. Unused J, K inputs should be tied to V_{CC}.

Logic levels to the J*, K* inputs should be stabilized to the logical ONE or ZERO level 15 ns before the clock pulse and should remain stable for 10 ns after the rise of the clock pulse. Unused J*, K* inputs must be tied to ground.

A logical ZERO on the P_J line sets the Q output to logic ONE. A logical ZERO on the clear line resets the Q output to logic ZERO. When the P_J and P_K lines are not activated they must be at a logic ONE level (or tied to V_{CC}). The P_J and P_K lines should not be activated while the clock line is at the logic ONE level.

Inverting and gated inputs reduce system can count for many applications.

6A



Component values shown are typical.

TRUTH TABLE

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$P_K = 0 \Longrightarrow Q = 0$

a capacitively-coupled, high-speed, J-K flip-flop lly for shifting and counting operating in systems clock pulse rates in the order of 30 MHz. It is well suited to general applications in high-speed systems.

Outputs of the Signetics NE826A employ active pull-up to effect low signal transition times when driving capacitive loads as in "Ripple Counters."

An asynchronous input is provided to allow the flip-flop to be cleared independently of the state of the clock pulse input.

The NE826A is triggered by the falling (negative-going) edge of the clock pulse waveform.

ELECTRICAL CHARACTERISTICS: NE806, NE808, NE816, NE840, NE855, NE870, NE880 (Notes: 1,2,3,4,5

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	GUARANTEES				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNITS	TEMP.	V_{CC}	DRIVEN INPUT	ALL OTHER INPUTS	OUTPUT	NOTES
A-5	**"I" OUTPUT VOLTAGE**	2.4	2.8		V	0°C	4.5 V	0.8 V		−400 μA	8, 12
A-3		2.4	3.1		V	+25°C	4.5 V	0.8 V		−400 μA	8
A-4		2.4	3.5		V	+70°C	4.5 V	0.8 V		−400 μA	8
A-5	**"0" OUTPUT VOLTAGE**		0.20	0.40	V	0°C	4.5 V	2.0 V	2.0 V	16 mA	9, 13
A-3			0.20	0.40	V	+25°C	4.5 V	2.0 V	2.0 V	16 mA	9, 13
A-4			0.25	0.40	V	+70°C	4.5 V	2.0 V	2.0 V	16 mA	9, 13
C-1	**"0" INPUT CURRENT**			−1.6	mA	0°C	5.5 V	0.4 V	OPEN		
A-3				−1.6	mA	+25°C	5.5 V	0.4 V	OPEN		
C-1				−1.6	mA	+70°C	5.5 V	0.4 V	OPEN		
C-1	**"I" INPUT CURRENT**		2	40	μA	0°C	5.5 V	4.5 V	0 V		
A-3			2	40	μA	+25°C	5.5 V	4.5 V	0 V		
A-4			2	40	μA	+70°C	5.5 V	4.5 V	0 V		
A-6	**TURN-ON DELAY** (Fig. 1)		8	15	ns	+25°C	5.0 V			F.O.=MAX.	
A-6	**TURN-OFF DELAY** (Fig. 1)		18	29	ns	+25°C	5.0 V			F.O.=1	
C-2	**INPUT CAPACITANCE**		2.0	3.0	pf	+25°C	5.0 V	2.0 V			
	POWER DISSIPATION NE808, NE816, NE870, NE880										
A-2	OUTPUT "I"		5		mW	+25°C	5.0 V	0 V			
A-2	OUTPUT "0"		15		mW	+25°C	5.0 V	5.0 V			7
	NE840										
A-2	OUTPUT "I"		10		mW	+25°C	5.0 V	0 V			
A-2	OUTPUT "0"		19		mW	+25°C	5.0 V	5.0 V			
	NE855										
A-2	OUTPUT "I"		10		mW	+25°C	5.0 V	0 V			
A-2	OUTPUT "0"		43		mW	+25°C	5.0 V	5.0 V			
	DC FANOUT										
	NE808, NE816, NE870, NE880	10									
	NE840	10									
	NE855	30									
A-2	**INPUT LATCH VOLTAGE**	6.0			V	+25°C	5.0 V	10 mA	0 V		16
A-2	**OUTPUT SHORT CIRCUIT CURRENT**	20		70	mA	+25°C	5.5 V	0 V		0 V	

NOTES:

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

(2) All measurements are taken with pin 11 tied to zero volts.

(3) Positive current flow is defined as into the terminal referenced.

(4) Positive NAND Logic Definition: "UP" Level="1", "DOWN" Level="0".

(5) Precautionary measures should be taken to insure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.

(6) Measurements apply to each gate element independently.

(7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f=1 Mc, V=25 mV_{RMS}. All pins not specifically referenced are tied to guard for capacitance tests. Any fan-in expansion nodes are open.

(8) Output source current is supplied through a 6KΩ resistor to ground.

(9) Output sink current is supplied through a 256Ω resistor to V_{CC}.

(10) Power dissipation per gate.

(11) Measurement made with 10% duty cycle.

(12) NE855 guarantee with output source current of −1.2 mA through a 2KΩ resistor to ground.

(13) NE855 guarantee with output sink current of 48 mA through an 85Ω resistor to V_{CC}.

(14) Input current measurements on J_1, J_2, require J*=Clock=Ground and momentarily ground clear. Input current measurements on K_1, K_2 require K*=Clock=Ground and momentarily ground preset.

(15) Input current measurements on preset and clear require J*=K*=Ground.

(16) Measurement insures that minimum latch voltage is greater than maximum V_{CC}.

ELECTRICAL CHARACTERISTICS: NE825A (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	GUARANTEES				TEST CONDITIONS							
		MIN.	TYP.	MAX.	UNITS	TEMP.	V_{CC}	PRESET	CLEAR	CLOCK	DRIVEN INPUT	OUTPUT	NOTES
A-5	**"1" OUTPUT VOLTAGE (Q)**	2.4	2.8		V	0°C	4.5 V	0.8 V	2.0 V	0 V		−400 μA	8
A-3		2.4	3.1		V	+25°C	4.5 V	0.8 V	2.0 V	0 V		−400 μA	8
A-4		2.4	3.5		V	+70°C	4.5 V	0.8 V	2.0 V	0 V		−400 μA	8
A-5	**"1" OUTPUT VOLTAGE ($\overline{Q}$)**	2.4	2.8		V	0°C	4.5 V	2.0 V	0.8 V	0 V		−400 μA	8
A-3		2.4	3.1		V	+25°C	4.5 V	2.0 V	0.8 V	0 V		−400 μA	8
A-4		2.4	3.5		V	+70°C	4.5 V	2.0 V	0.8 V	0 V		−400 μA	8
A-5	**"0" OUTPUT VOLTAGE (Q)**		0.20	0.40	V	0°C	4.5 V	2.0 V	0.8 V	0 V		16 mA	9
A-3			0.20	0.40	V	+25°C	4.5 V	2.0 V	0.8 V	0 V		16 mA	9
A-4			0.25	0.40	V	+70°C	4.5 V	2.0 V	0.8 V	0 V		16 mA	9
A-5	**"0" OUTPUT VOLTAGE ($\overline{Q}$)**		0.20	0.40	V	0°C	4.5 V	0.8 V	2.0 V	0 V		16 mA	9
A-3			0.20	0.40	V	+25°C	4.5 V	0.8 V	2.0 V	0 V		16 mA	9
A-4			0.25	0.40	V	+70°C	4.5 V	0.8 V	2.0 V	0 V		16 mA	9
C-1	**"0" INPUT CURRENT**			1.6	mA	0°C	5.5 V	OPEN	OPEN		0.4 V		14
A-3	**J_1, J_2, J*, K_1, K_2, K*, CLOCK**			1.6	mA	+25°C	5.5 V	OPEN	OPEN		0.4 V		14
C-1				1.6	mA	+70°C	5.5 V	OPEN	OPEN		0.4 V		14
C-1	**PRESET, CLEAR**			3.2	mA	0°C	5.5 V			0 V	0.4 V		15
A-3				3.2	mA	+25°C	5.5 V			0 V	0.4 V		15
C-1				3.2	mA	+70°C	5.5 V			0 V	0.4 V		15
C-1	**"1" INPUT CURRENT**		2	40	μA	0°C	5.5 V				4.5 V		
A-3	**J_1, J_2, J*, K_1, K_2, K*, CLOCK**		2	40	μA	+25°C	5.5 V				4.5 V		
A-4			2	40	μA	+70°C	5.5 V				4.5 V		
	PRESET, CLEAR		4	80	μA	0°C	5.5 V			0 V	4.5 V		
			4	80	μA	+25°C	5.5 V			0 V	4.5 V		
			4	80	μA	+70°C	5.5 V			0 V	4.5 V		
-6	**TURN-ON DELAY** (Fig. 2)		30	50	ns	+25°C	5.0 V					F.O.=10	
	TURN-OFF DELAY (Fig. 2)		30	50	ns	+25°C	5.0 V					F.O.=1	
	MINIMUM INPUT SET-UP TIME (Fig. 2)		15		ns	+70°C	5.0 V						
	MINIMUM INPUT HOLD TIME (Fig. 2)		10		ns	+25°C	5.0 V						
2	**INPUT CAPACITANCE J_1, J_2, J*, K_1, K_2, K*, CLOCK**		2.0	3.0	pf	+25°C	5.0 V				2.0 V		7
	PRESET, CLEAR		4.0	6.0	pf	+25°C	5.0 V				2.0 V		7
A-2	**POWER DISSIPATION**		70		mW	+25°C	5.0 V						
A-2	**INPUT LATCH VOLTAGE J_1, J_2, J*, K_1, K_2, K*, CLOCK, PRESET, CLEAR**	6.0			V	+25°C	5.0 V				10 mA		16
	OUTPUT SHORT CIRCUIT												
	CURRENT (Q)	20		70	mA	+25°C	5.5 V	0 V		0 V		0 V	
A-2	CURRENT ($\overline{Q}$)	20		70	mA	+25°C	5.5 V		0 V	0 V		0 V	

SEE NOTES ON PRECEEDING PAGE

ELECTRICAL CHARACTERISTICS: NE826A (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	GUARANTEES				TEST CONDITIONS							
		MIN.	TYP.	MAX.	UNITS	TEMP.	V_{CC}	P_K	CLOCK	J	K	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q_1, Q_2)	2.4	3.0		V	0°C	4.5 V		CLOCK	2.1 V	0.7 V	−200 μA	7,
A-3		2.4	3.1		V	+25°C	4.5 V		CLOCK	2.1 V	0.7 V	−200 μA	7,
A-4		2.4	3.3		V	+70°C	4.5 V		CLOCK	2.1 V	0.7 V	−200 μA	7, 12
A-5	"1" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)	2.4	3.0		V	0°C	4.5 V	0.7 V				−200 μA	7
A-3		2.4	3.1		V	+25°C	4.5 V	0.7 V				−200 μA	7
A-4		2.4	3.3		V	+70°C	4.5 V	0.7 V				−200 μA	7
A-5	"0" OUTPUT VOLTAGE (Q_1, Q_2)		0.2	0.4	V	0°C	4.5 V	0.7 V				8.0 mA	8
A-3			0.2	0.4	V	+25°C	4.5 V	0.7 V				8.0 mA	8
A-4			0.2	0.4	V	+70°C	4.5 V	0.7 V				8.0 mA	8
A-5	"0" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)		0.2	0.4	V	0°C	4.5 V		CLOCK	2.1 V	0.7 V	8.0 mA	8, 12
A-3			0.2	0.4	V	+25°C	4.5 V		CLOCK	2.1 V	0.7 V	8.0 mA	8, 12
A-4			0.2	0.4	V	+70°C	4.5 V		CLOCK	2.1 V	0.7 V	8.0 mA	8, 12
A-3	"0" INPUT CURRENT J_1, K_1, J_2, K_2			−2.4	mA	+25°C	5.5 V			0.4 V	0.4 V		
A-3	"0" INPUT CURRENT P_{K_1}, P_{K_2}			−1.9	mA	+25°C	5.5 V	0.4 V					
A-3	"0" INPUT CURRENT C_{P_1}, C_{P_2} (CLOCK)			−10	μA	+25°C	5.5 V		0.4 V				
A-3	"1" INPUT CURRENT		10	40	μA	+25°C	5.5 V	4.5 V		4.5 V	4.5 V		1
A-4	J_1, J_2, K_1, K_2, P_{K_1}, P_{K_2}		10	40	μA	+70°C	5.5 V	4.5 V		4.5 V	4.5 V		1
A-3	"1" INPUT CURRENT			10	μA	+25°C	5.5 V		4.5 V				
A-4	C_{P_1}, C_{P_2} (CLOCK)			10	μA	+70°C	5.5 V		4.5 V				
A-2	POWER CONSUMPTION		32		mW	+25°C	5.0 V						
A-2	OUTPUT SHORT CIRCUIT CURRENT Q_1, Q_2	−20		−70	mA	+25°C	5.0 V	0 V				0 V	
A-2	INPUT LATCH VOLTAGE J_1, J_2, K_1, K_2, P_{K_1}, P_{K_2} C_{P_1}, C_{P_2}	6.0			V	+25°C	5.0 V	10 mA	10 mA	10 mA	10 mA		9,
	TURN-ON DELAY		17		ns	+25°C	5.0 V					F.O.=	
	TURN-OFF DELAY		10		ns	+25°C	5.0 V					F.O.=	
	TOGGLE RATE (Fig. 3)		25		MHz	+25°C	5.0 V						
	INPUT CAPACITANCE J_1, J_2, K_1, K_2, P_{K_1}, P_{K_2}		2.0		pf	+25°C		2.0 V		2.0 V	2.0 V		
	INPUT CAPACITANCE C_{P_1}, C_{P_2} (CLOCK)		50		pf	+70°C			2.0 V				11

NOTES:

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

(2) All measurements are taken with pin 11 tied to zero volts.

(3) Positive current flow is defined as into the terminal referenced.

(4) Positive NAND Logic Definition: "UP" Level="1", "DOWN" Level="0".

(5) Precautionary measures should be taken to insure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.

(6) Measurements apply to each binary element independently.

(7) Output source current is supplied through a 12K resistor to ground.

(8) Output sink current is supplied through a resistor to V_{CC}.

(9) This test guarantees latch free operation over the specified operating power supply range.

(10) Recommended Clock Pulse Limits: Clock Pulse Amplitude=2.4 V min. 15 ns min., t_r=2 ns min., t_f=20 ns max. Signal levels at the (J and K) should be settled before the clock pulse rises.

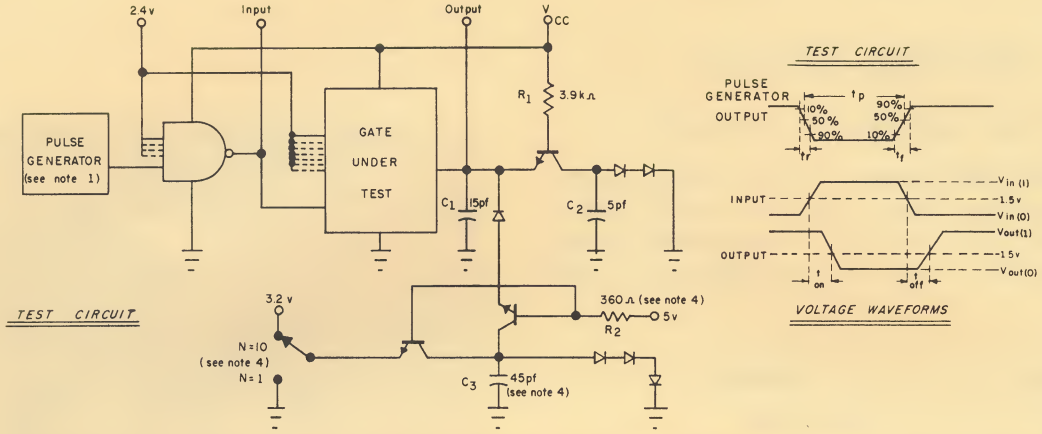
(11) Capacitance is measured on Boonton Electronic Corporatio Capacitance Bridge or equivalent, f=1.0 MHz, V_{AC}=25 mV specifically referenced are tied to guard for capacitance tes

(12) The binary Q output is set to "1" by clocking once with and K input low. Clock Pulse Requirement: Clock Pulse Amp...e=2.4 v; Clock Pulse Width=100 ns; t_r=t_f=10 ns. For alternate Q test, apply P_K=0.7V.

(13) To test "1" Input Current for J, P_K, set Q="0". To test "1" Input Current for K, set $\bar{Q}$="0".

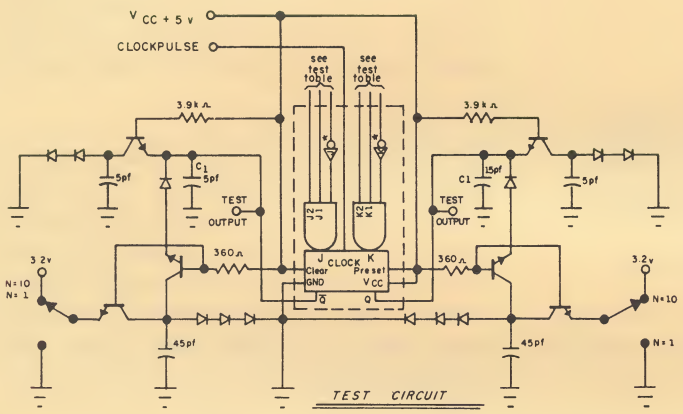
(14) To test Input Latch Voltage at P_K input, set Q="0".

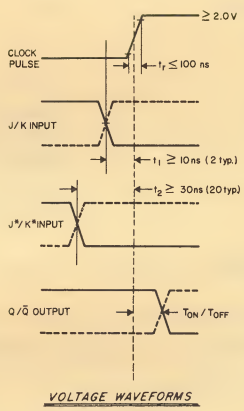
FIGURE 1 — GATE PROPAGATION DELAY



NOTES: (1) The generator has the following characteristics: $t_r = t_f \leq 10$ nsec, $t_p = 100$ nsec, PRR = 1 Mc, $Z_{out} \approx 50\ \Omega$.
(2) All transistors are 2N2368.
(3) All diodes are 1N916.
(4) Test NE855 with $R_2 = 100\ \Omega$, $C_3 = 145$ pf, N = 30 for t_{on}, and N = 1 for t_{off}.
(5) $t_{pd} = \frac{t_{on} + t_{off}}{2}$

FIGURE 2 — NE825A SWITCHING TIME

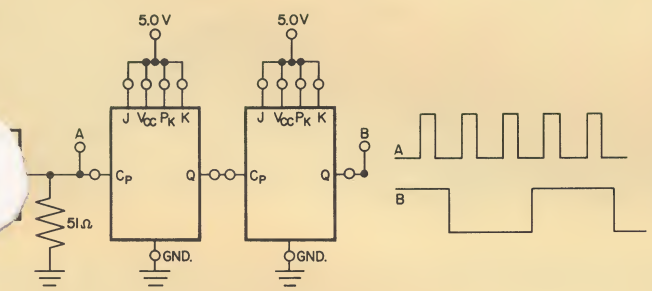


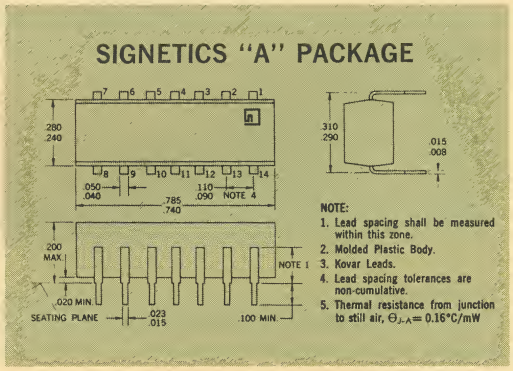


TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	+2.4 v	GND
1	t_{on} ($\bar{Q}$)	J*	J1, J2	K1, K2	K*
2	t_{off} ($\bar{Q}$)	K*	K1, K2	J1, J2	J*
3	t_{on} (Q)	K*	K1, K2	J1, J2	J*
4	t_{off} (Q)	J*	J1, J2	K1, K2	K*

NOTES: (1) All transistors are 2N2368.
(2) All diodes are 1N916.

FIGURE 3 — TOGGLE RATE TEST CIRCUIT — NE826A





NE800A-SERIES

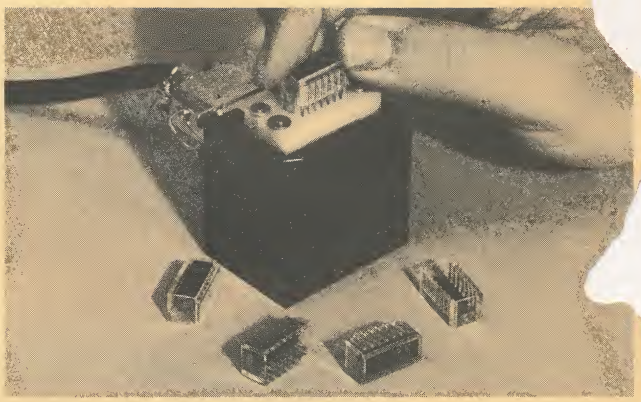
RELIABILITY OF SIGNETICS "A" PACKAGE

The Signetics solid molded package is capable of meeting or exceeding all of the moisture resistance requirements specified in MIL-S-19500 and MIL-STD-750. Furthermore, it meets or exceeds all other key mechanical, environmental and life test requirements of those specifications.

Test	Conditions
Solderability	All terminals
Temp Cycling	10 Cycles, T=+125°C
Thermal Shock	5 cycles, 1 minute at each extreme 0°C and +100°C, transfer time= 5 sec max
Moisture Resistance	Polarized and non-polarized
Shock	1500 g; 5 blows y_1; 0.5 msec
Vibration, Fatigue	30 g; non-operating
Vibration, Variable Frequency	30 g
Acceleration	30,000 g; 1 min. y_1
Operating Life	1000 hours at T_{min}=+85°C, dynamic operation at 100 KHz
Storage Life	1000 hours at T_{min}=+125°C

"A" PACKAGE CARRIER AND TEST SYSTEM

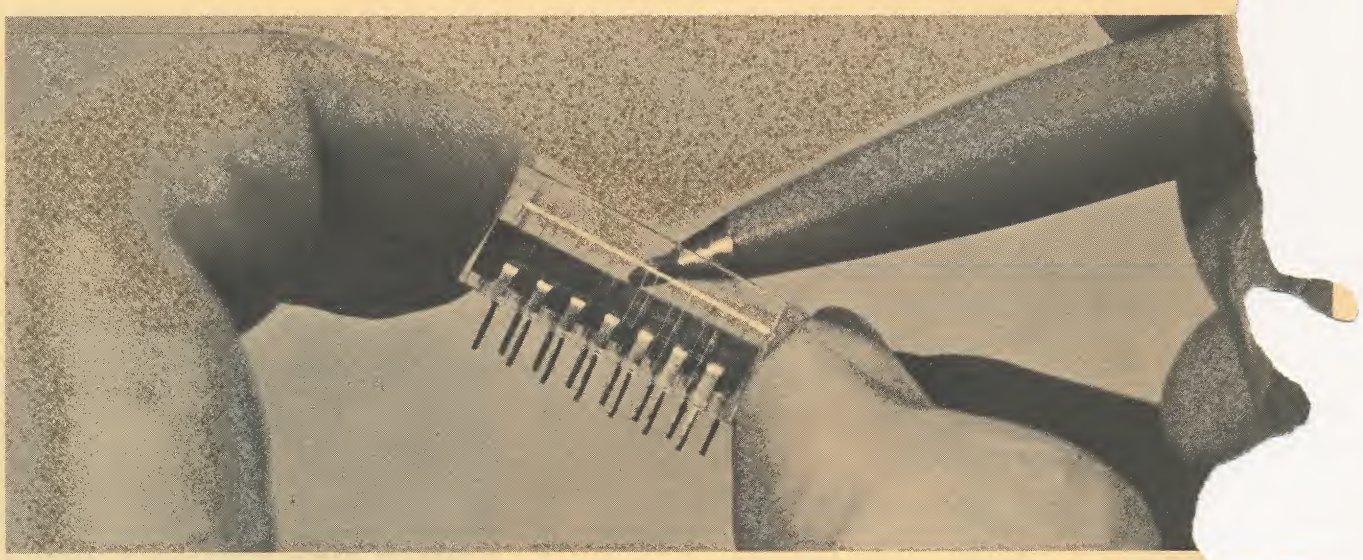
The carrier designed for the Signetics "A" package is a multi-purpose device that functions in shipping, handling, testing and assembly of finished modules.



SIGNETICS MODEL GT-03 TEST HEAD

The GT-03 Contactor is designed to mate with the "A" package leads while the package is contained in the carrier. It thus provides a rapid and reliable means for making electrical contact with the device leads during testing without damage to the leads. The GT may be utilized in conjunction with test equipment for inco inspection, engineering evaluation and other testing requirem Consult the factory for specifications, price and delivery informa

As shown, the grooved plastic carrier protects the device l against bending and mis-alignment. The carrier also serve assembly alignment jig for insertion of the package into a circuit board. The package is pushed slightly out of the c expose the package leads which are then registered with t in the PC board. The package is then firmly pushed into pl leads springing to a slightly wider position, holding the pac against the PC board. The carrier is then discarded.



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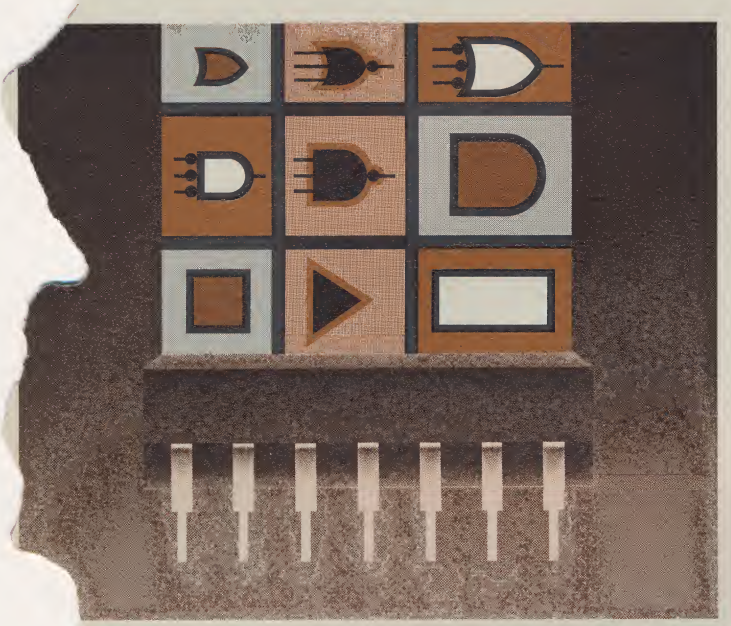
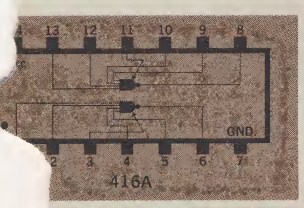
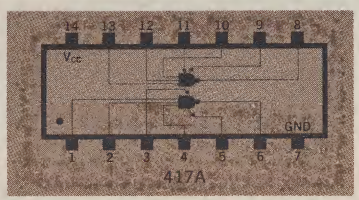
TRANSISTOR TRANSISTOR LOGIC

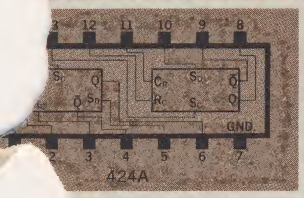
INDUSTRIAL

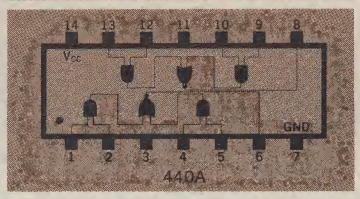
SP400 SERIES +15° C to +55° C
ST400 SERIES 0° C to +70° C

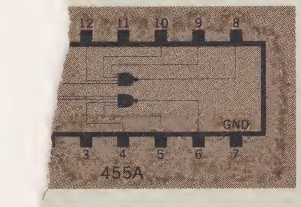


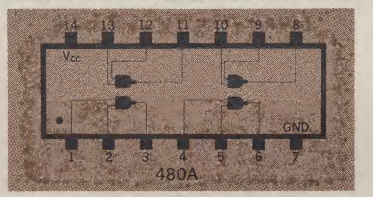


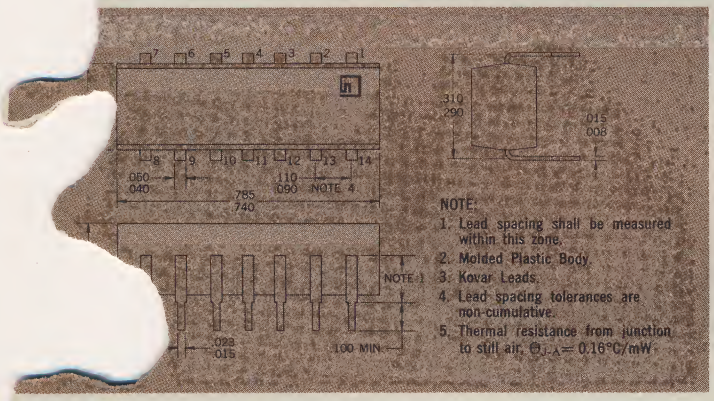












SP416A, ST416A, Dual 4-Input Expandable NAND Gate

SP417A, ST417A, Dual 3-Input Expandable NAND Gate

SP424A, ST424A, Dual AC Binary Element

SP440A, ST440A, Dual Exclusive OR Gate

SP455A, ST455A, Dual 4-Input Power Gate

SP480A, ST480A, Quad 2-Input NAND Gate

The Signetics 400A family is a compatible set of logic elements in which the more desirable characteristics of both DTL and TTL have been utilized with emphasis on low power consumption, high reliability and low cost. All of the elements are fabricated within monolithic silicon substrates through use of planar and epitaxial techniques. Low system can count is provided by the variety of logic elements including a dual binary and by the high fan-out of the elements.

The family is made available in two operating temperature ranges, +15°C to +55°C for the SP series and 0°C to +70°C for the ST series, in order to allow the system designer wide latitude in system cost/environment trade-offs.

When operated at the preferred power supply value of 5.0 volts, and within the specified temperature range, the 400A series offers the following system advantages:

- **HIGH NOISE MARGIN** — 700 mV to 1.5 V
- **LOW POWER CONSUMPTION** — 9.0 mW
- **LOW SYSTEM CAN COUNT** — Dual Binary
- **HIGH FAN-OUT** — 7

The solid molded dual in-line package used in the 400A series is unique in integrated circuit packaging in that the molding process makes a monolithic structure of the circuit chip, the internal wires, and the external leads. The simplicity of the package provides inherently low cost in both manufacturing and subsequent handling by the user, as well as very reliable performance under severe environmental conditions. Extensive reliability data based on nearly two years of testing this package is available on request to Signetics Technical Information Center.

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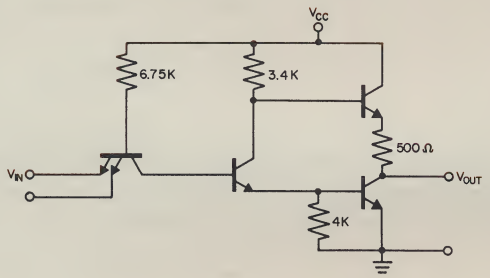
TABLE I — ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Element	Input Voltage	Output Voltage	V_{cc}	Input Current	Output Current	Node Input Current	Power Dissipation
SP416A, ST416A	+5.5V	+6.0V	+6.0V	±30mA	+100, -20mA	±20mA	150mW
SP417A, ST417A	+5.5V	+6.0V	+6.0V	±30mA	+100, -20mA	—	150mW
SP424A, ST424A	+5.5V	+6.0V	+6.0V	±10mA	+100, -20mA	—	150mW
SP440A, ST440A	+5.5V	+6.0V	+6.0V	±30mA	+100, -20mA	—	150mW
SP455A, ST455A	+5.5V	+6.0V	+6.0V	±30mA	+150, -20mA	—	150mW
SP480A, ST480A	+5.5V	+6.0V	+6.0V	±30mA	+100, -20mA	—	150mW

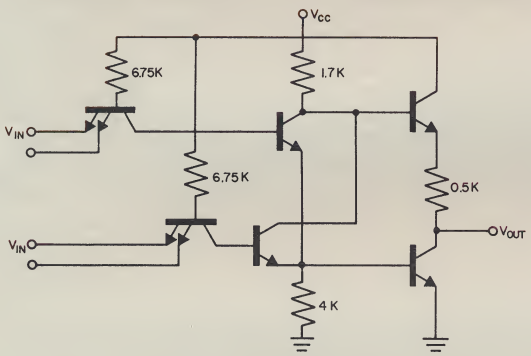
GATE — 480A



NOTE: ¼ of 480A shown. Component values are typical.

The 480A utilizes multiple emitter transistor (M... inputs and push-pull or totem pole outputs character-istic of TTL logic circuitry. Relatively high speed and good capacitive drive capability is provided by this gate. Propagation delay, rise time and fall time are relatively independent of load. Power consump-tion is relatively constant with increasing frequency of operation since both output transistors are never in the "ON" condition simultaneously. Each input constitutes one DC load.

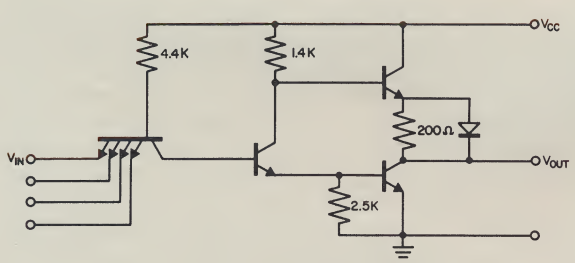
EXCLUSIVE OR GATE — 440A



NOTE: ½ of 440A shown. Component values are typical

The 440A is a dual two-input AND-OR Inve... which may be used to implement the EXCLUSIV... function. The 440A exhibits the general charac... tics of the 480A gate circuit and is suited for ap... tion in digital comparators, half or full adde... general AND-OR control logic functions to the ... of the 424A binary.

POWER GATE — 455A



NOTE: ½ of 455A shown. Component values are typical.

The 455A is a dual 4-input power NAND gate inten... specifically for driving clock lines or other h... -pacitance loads. The output structure of th... incorporates a parallel resistor-diode combi... for optimum capability of fast rise time while driv... into a large capacitance.

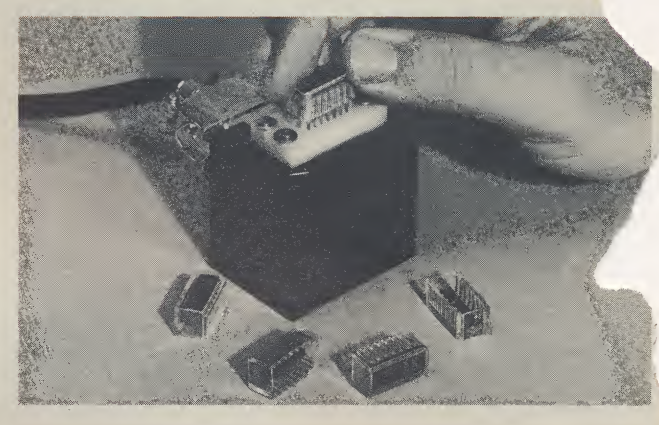
RELIABILITY OF SIGNETICS "A" PACKAGE

The Signetics solid molded package is capable of meeting or exceeding all of the moisture resistance requirements specified in MIL-S-19500 and MIL-STD-750. Furthermore, it meets or exceeds all other key mechanical, environmental and life test requirements of those specifications.

Test	Conditions
Solderability	All terminals
Temp Cycling	10 Cycles, T=+125°C
Thermal Shock	5 cycles, 1 minute at each extreme, 0°C and +100°C, transfer time= 5 sec max
Moisture Resistance	Polarized and non-polarized
Shock	1500 g; 5 blows y_1; 0.5 msec
Vibration, Fatigue	30 g; non-operating
Vibration, Variable Frequency	30 g
Acceleration	30,000 g; 1 min. y_1
Operating Life	1000 hours at T_{min}=+85°C, dynamic operation at 100 KHz
Storage Life	1000 hours at T_{min}=+125°C

"A" PACKAGE CARRIER AND TEST SYSTEM

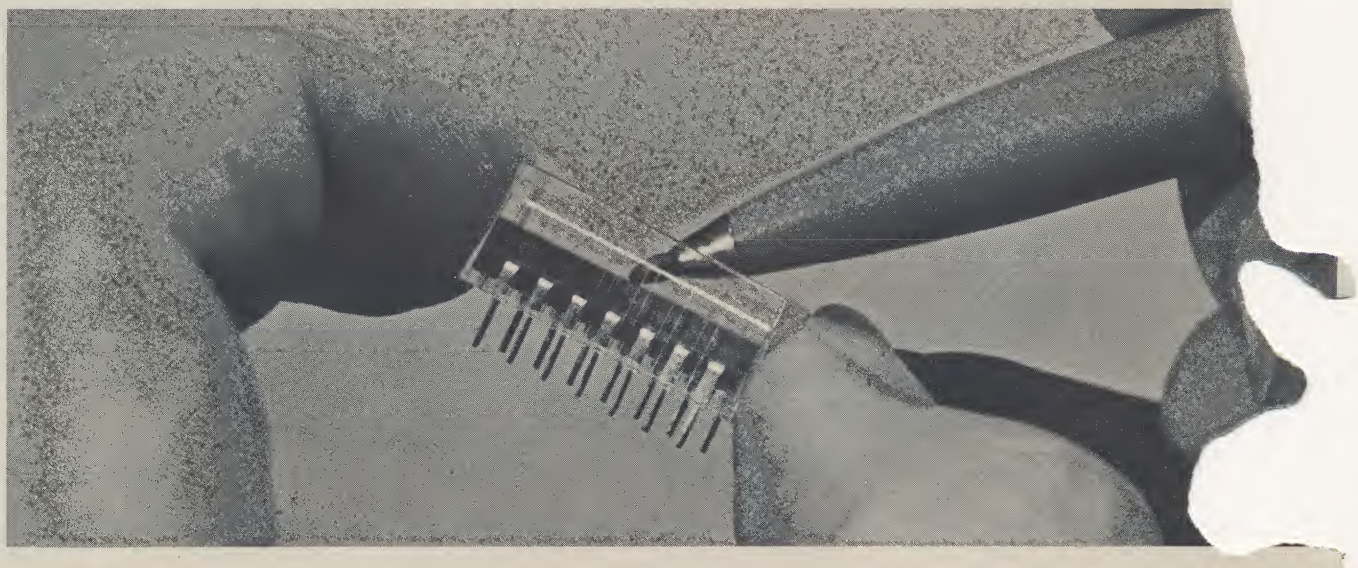
The carrier designed for the Signetics "A" package is a multi-purpose device that functions in shipping, handling, testing and assembly of finished modules.



SIGNETICS MODEL GT-03 TEST HEAD

The GT-03 Contactor is designed to mate with the "A" package leads while the package is contained in the carrier. It thus provides a rapid and reliable means for making electrical contact with the device leads during testing without damage to the leads. The G may be utilized in conjunction with test equipment for inc inspection, engineering evaluation and other testing requiren Consult the factory for specifications, price and delivery inform

As shown, the grooved plastic carrier protects the devi against bending and mis-alignment. The carrier also ser assembly alignment jig for insertion of the package into circuit board. The package is pushed slightly out of the expose the package leads which are then registered with in the PC board. The package is then firmly pushed into pla leads springing to a slightly wider position, holding the package against the PC board. The carrier is then discarded.



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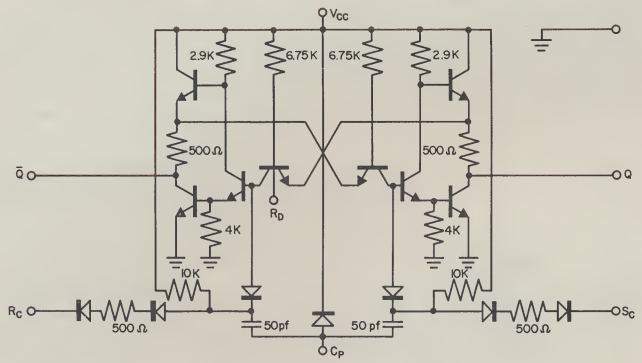
RS/T DUAL FLIP-FLOP — 424A



NOTE: ½ of 424A shown. Component values are typical.

TRUTH TABLE

R_C	S_C	Q_{N+1}
1	0	1
0	1	0
1	1	No Change
0	0	?

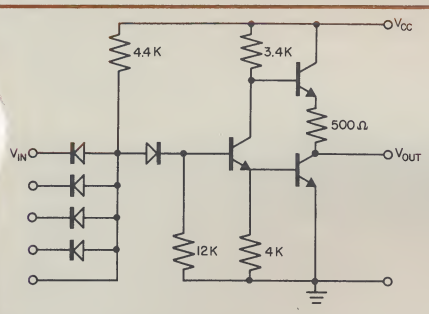
$R_D = 0 \Longrightarrow Q = 0$

The 424A is a dual AC (capacitively-coupled) RS/T flip-flop capable of toggling at 9 MHz. The two flip-flops are completely independent, having common connections only to the power supply and ground. A protective diode is included at each clock input to limit positive excursions of the clock line to about 0.5 volt above the power supply and negative excursions to about 30 volts. The current in this diode should be limited to 1.0mA maximum. The truth table for the 424A is shown above (positive logic assumed, high logic level = 1). This table, of course, applies only at clock time. The S and R inputs have no effect when the clock line is stationary. If S and R inputs are both low at clock time, the new state of the flip-flop cannot be determined; therefore, this condition must be prevented from ever occurring. This may be accomplished by including the outputs of the flip-flop as additional inputs to the gates which drive the S and R inputs. S and R inputs represent a load of 0.4mA; however, when the clock line rises, additional transient current flows out of the enabling input which is in the "0" state. Conservative design practice would require that S and R inputs be considered as 1.5 loads to allow for this transient current.

The clock pulse must have a minimum width of 100 nanoseconds, a minimum amplitude of 2.5 volts and a maximum fall time of 100 nanoseconds. Rise time of the pulse is not critical. S and R inputs should be settled at their final values before the clock line rises, so the best choice of clock pulse shape would be a low riding signal rising for only slightly more than the required minimum time. The flip-flop changes state on the falling edge of the clock pulse.

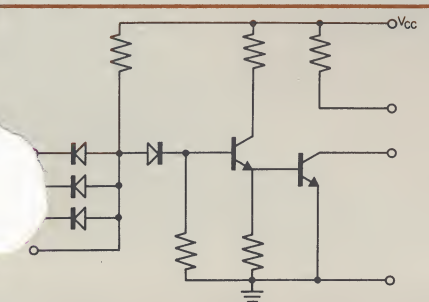
Preset inputs represent one standard load. The flip-flop changes to ZERO asynchronously when the preset input is pulled down.

- 416A



OTE: ½ of 416A shown. Component values are typical.

GAT 417A



NOTE: ½ of 417A shown.

These devices provide high speed and high functional density at very low power consumption levels. Propagation time is typically 30 nanoseconds. The 417A gate may be used in collector logic configurations. No more than seven collectors should be connected together and total rated fan-out should be reduced by 3/4 fan-out for each added collector. The expander node may be used with Signetics SE106, NE106A and SP631A gate expander elements.

TABLE II — INTERFACE INFORMATION

Element	Output Capabilities		Driving Element Requirements
	High	Low	
SP416A, ST416A	Source 400μA	Sink 6.4mA	Sink 1.2mA, Source 10μA
SP424A, ST424A	Source 400μA	Sink 6.4mA	Sink 1.0mA, (R_C, S_C) Sink 0.7mA, (S_D) Effective Capacitance = 60 pf (Clock)
SP440A, ST440A	Source 400μA	Sink 6.4mA	Sink 1.2mA, Source 50μA
SP455A, ST455A	Source 1.2mA	Sink 26mA	Sink 1.2mA, Source 50μA
SP480A, ST480A	Source 400μA	Sink 6.4mA	Sink 0.9mA, Source 50μA

LOADING AND INTERFACING RULES

When 400A series elements are used to drive other 400A series elements the loading rules are as shown in Table III. These guarantees are applicable for a nominal +5.0 volt power supply with ±5 percent tolerance and an operating temperature range of +15°C to +55°C (SP400A) or 0°C to +70°C (ST400A). Maximum power is guaranteed with a 5.0 volt power supply, ambient temperature of 25°C and 50 percent duty cycle.

When 400A series elements interface with long lines or with any circuits other than those in the 400A family, the loading rules are best defined in terms of current sink and source capability as shown in Table II.

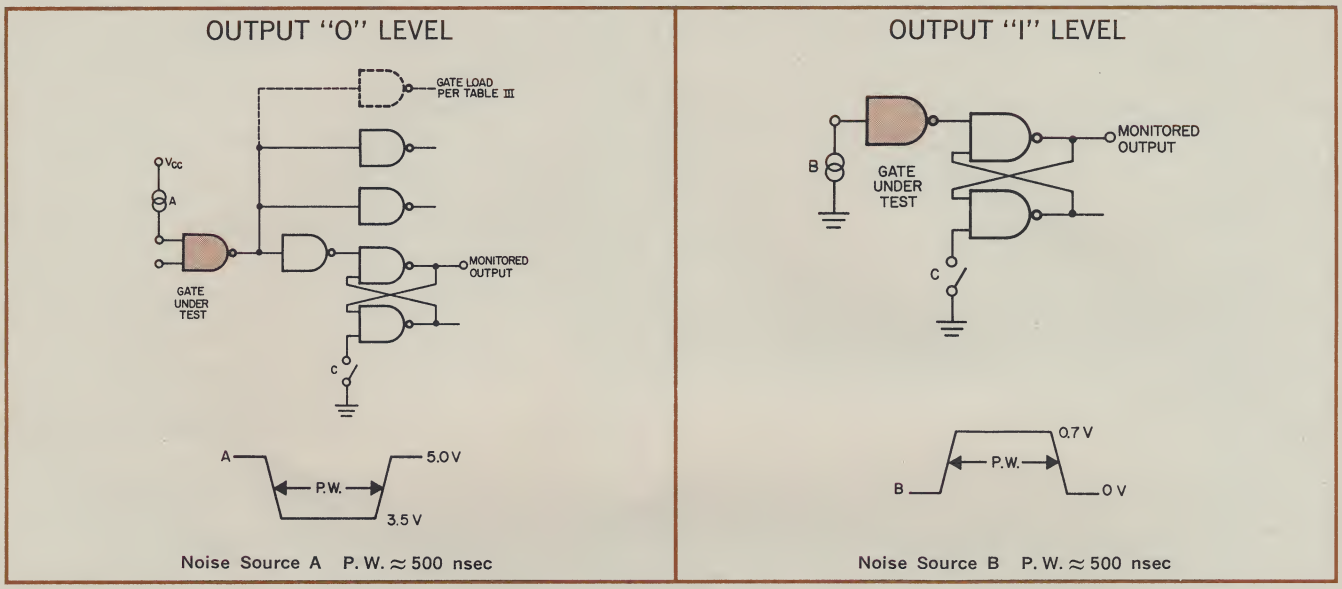
TABLE III — GUARANTEED LOADING CHART (V_{CC} = 5.0 Volts)

Driving Element	Maximum Power Per Function	Driven Input							
		SP416A ST416A	SP417A SP417A	SP424A, ST424A			SP440A ST440A	SP455A ST455A	SP480A ST480A
				S_D	S_C, R_C	C_P			
SP416A, ST416A	12mW	5	5	7	6	1	7	5	7
SP417A, ST417A	12mW	5	5	7	6	1	7	5	7
SP424A, ST424A	22mW	5	5	7	6	1	7	5	7
SP440A, ST440A	18mW	5	5	7	6	1	7	5	7
SP455A, ST455A	16mW	21	21	24	20	7	24	21	24
SP480A, ST480A	9.0mW	5	5	7	6	1	7	5	7

TABLE IV — GATE PAIR DELAY AND FLIP-FLOP TOGGLE RATE (V_{CC} = 5.0 V, T_A = 25°C)

Element	Maximum Pair Delay	Minimum Toggle Rate	Remarks
SP416A, ST416A	80 ns	—	Figure 3
SP417A, ST417A	80 ns	—	Figure 3
SP424A, ST424A	—	5.0 MHz	Figure 2
SP440A, ST440A	85 ns	—	Figure 3
SP455A, ST455A	85 ns	—	Figure 3
SP480A, ST480A	80 ns	—	Figure 3

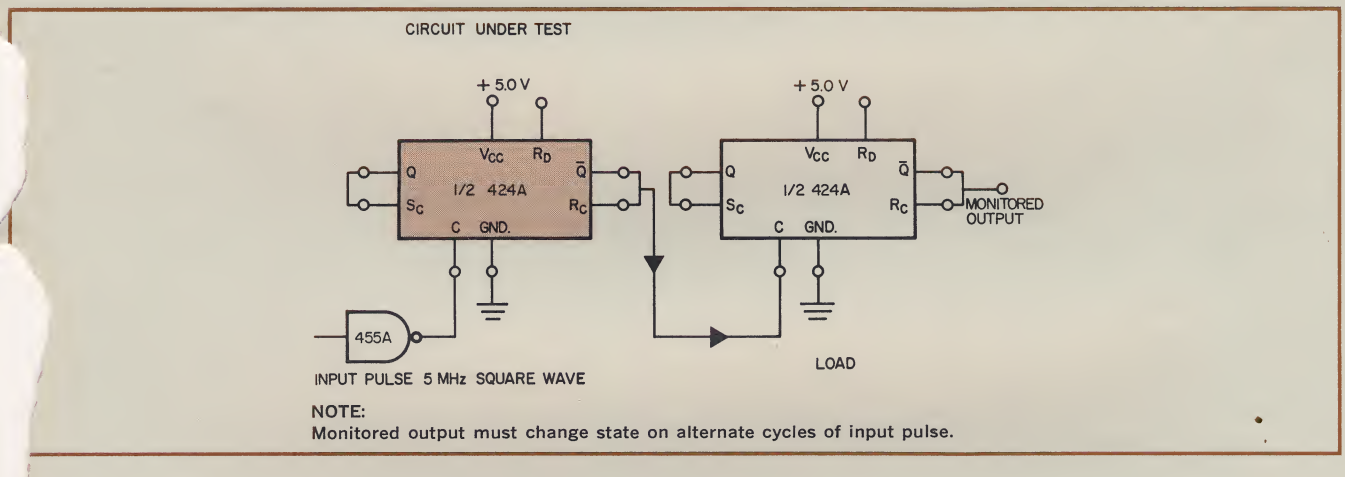
FIGURE 1 — NOISE MARGIN MEASUREMENTS



Noise margins in the 400A series elements may be expected to exceed 1.5 V from the "1" logic level, and 700mV from the "0" logic level. Noise margin measurements are made as shown in Figure 1. Guarantees for the SP400A series are applicable from +15°C to +55°C, and for the ST400A series from 0°C to +70°C. The measurement procedure is as follows:

(1) Momentarily close switch C to clear flip-flop.
(2) Apply the appropriate noise waveform.
(3) Flip-flop shall not change logical state at monitored output.
(4) Total fan-out gate loads are specified in the loading chart in Table III. Flip-flop is considered one gate load.

FIGURE 2 — TOGGLE RATE 424A



NOTE:
Monitored output must change state on alternate cycles of input pulse.

IGURE 3 — PAIR DELAY MEASUREMENTS